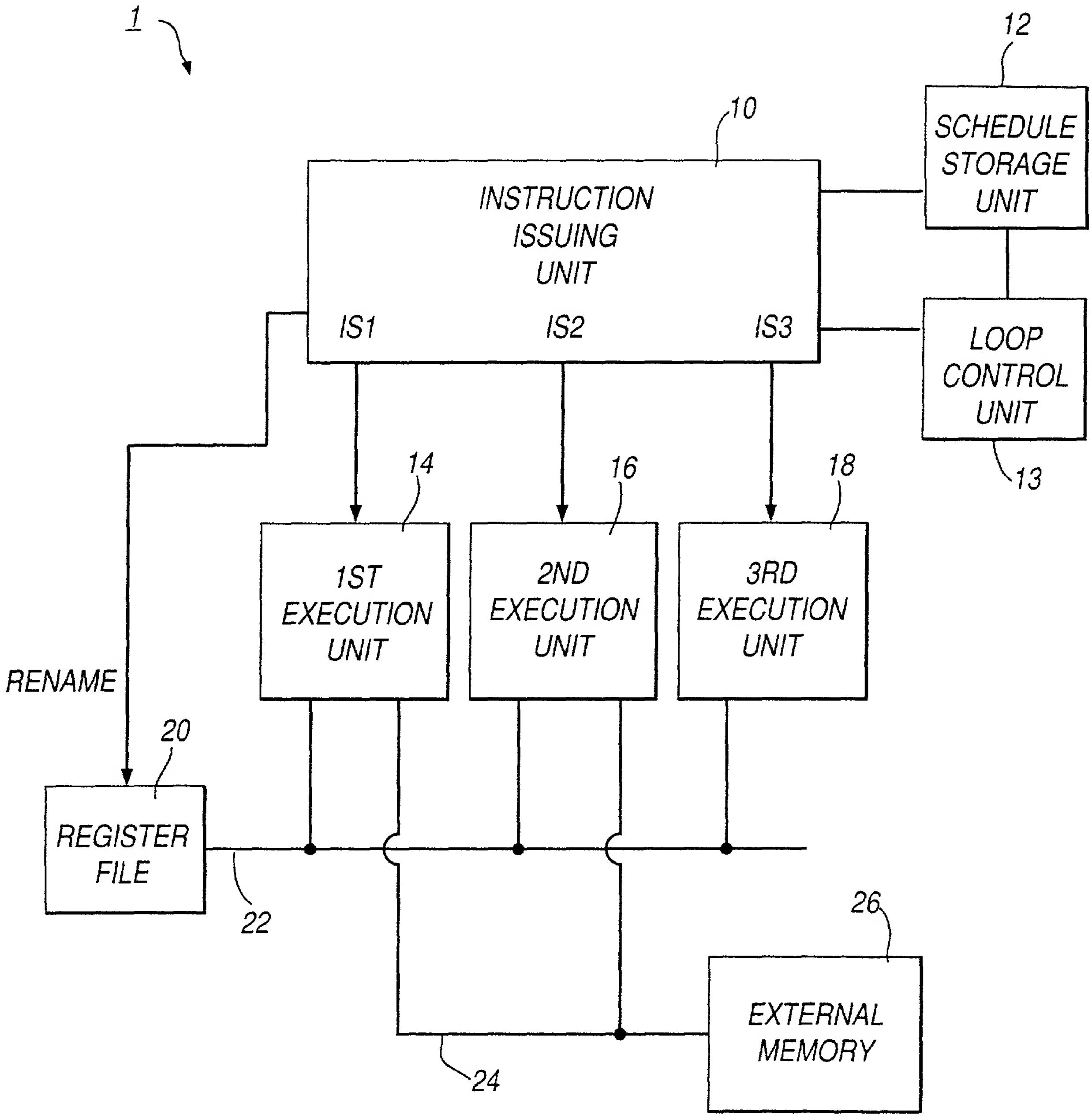

1
10
INSTRUCTION ISSUING UNIT
IS1
IS2
IS3
12
SCHEDULE STORAGE UNIT
LOOP CONTROL UNIT
13
14
16
18
1ST EXECUTION UNIT
2ND EXECUTION UNIT
3RD EXECUTION UNIT
RENAME
20
REGISTER FILE
22
26
EXTERNAL MEMORY
24

Fig.1

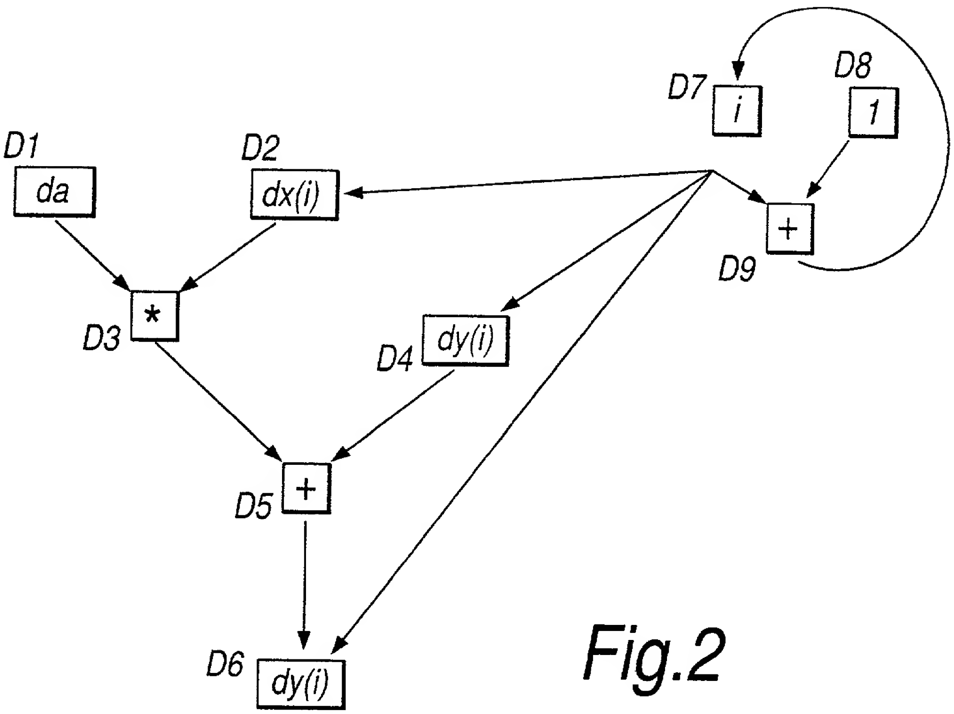

D1
da
D2
dx(i)
D7
i
D8
1
D9
+
D3
*
D4
dy(i)
D5
+
D6
dy(i)

Fig.2

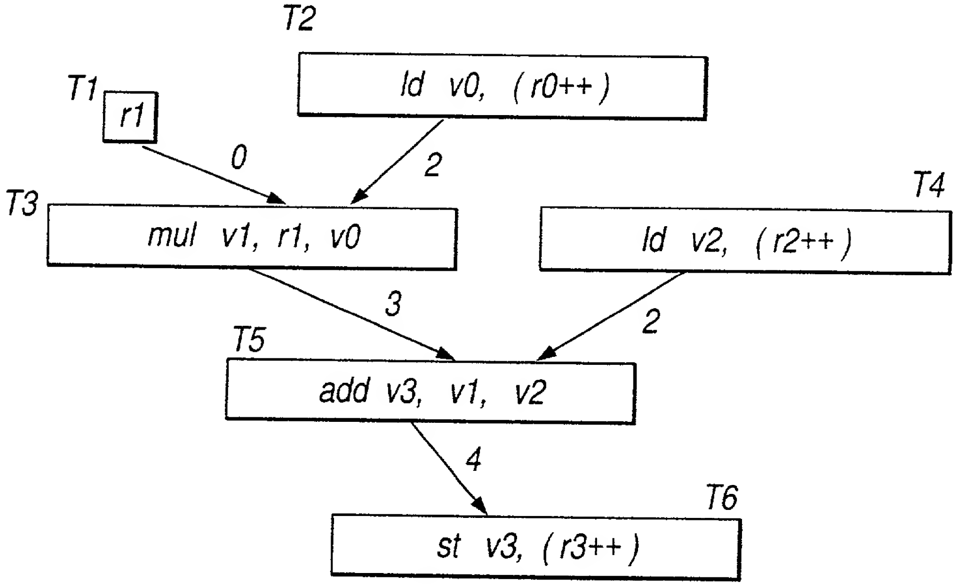

T2
ld v0, (r0++)
T1
r1
0
2
T3
mul v1, r1, v0
T4
ld v2, (r2++)
3
2
T5
add v3, v1, v2
4
T6
st v3, (r3++)

Fig.3

Stage	Cycle	Issue slot 1	Issue slot 2	Issue slot 3	v0	v1	v2	v3
1	0	ld v0, (r0++)			s0			
	1				s0			
2	2			mul v1, v0, r1	s1	s2		
	3	ld v2, (r2++)				s2	s4	
3	4					s3	s5	
	5			add v3, v1, v2		s3	s5	s6
4	6							s7
	7							s7
5	8							s8
	9		st v3, (r3++)					s8

Fig.4

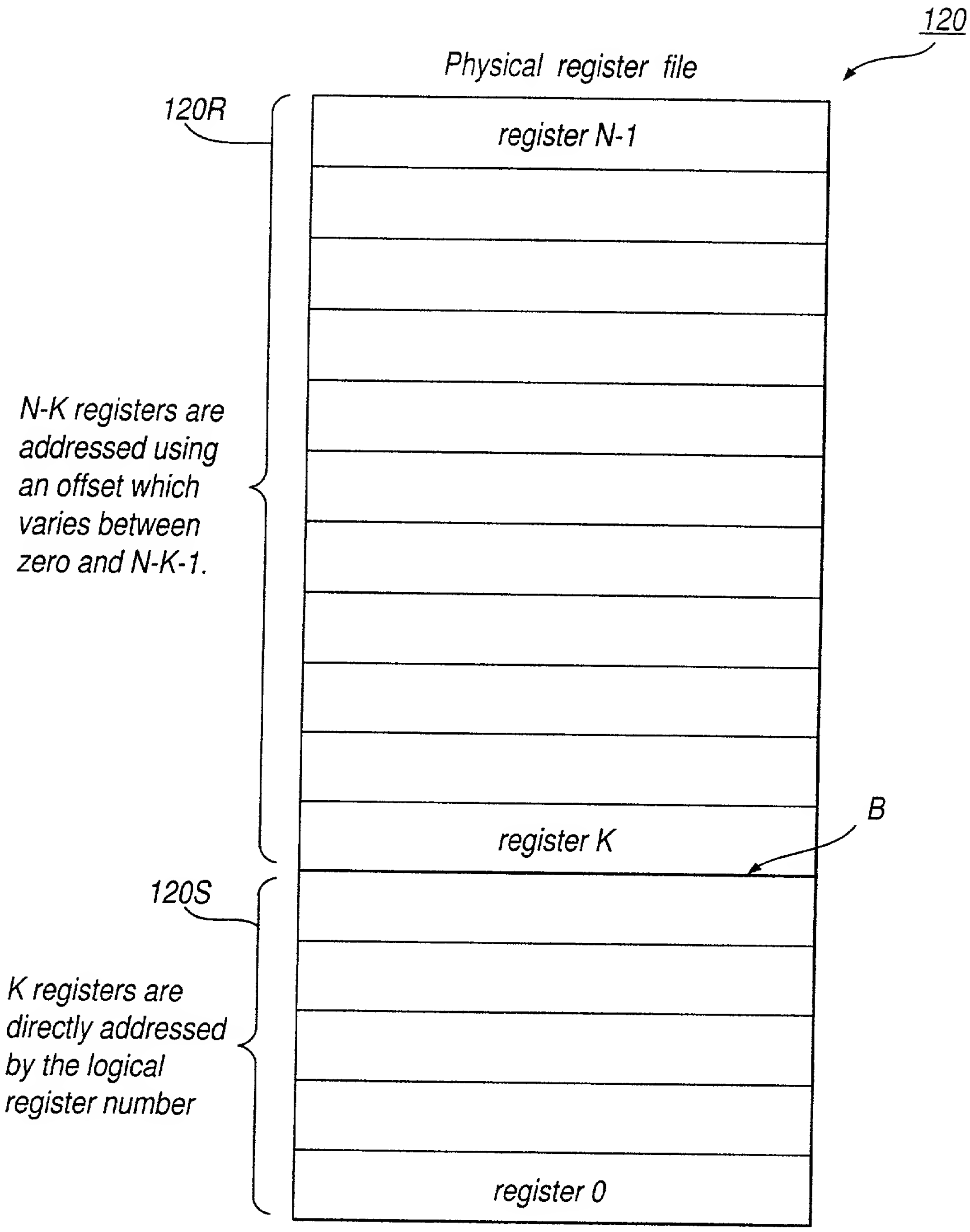

120
Physical register file
120R
register N-1
N-K registers are addressed using an offset which varies between zero and N-K-1.
register K
B
120S
K registers are directly addressed by the logical register number
register 0

Fig.5

		Iteration 0					Iteration 1				
Cycle	Offset	Instruction	v0	v1	v2	v3	Instruction	v0	v1	v2	v3
0	6	ld v0, (r0++)	r4 (▸ p10)								
1	6		r4 (▸ p10)								
2	5	mul v1, v0, r1	r5 (▸ p10)	r6 (▸ p11)			ld v0, (r0 ++)	r4 (▸ p9)			
3	5	ld v2, (r2++)		r6 (▸ p11)	r8 (▸ p13)			r4 (▸ p9)			
4	4			r7 (▸ p11)	r9 (▸ p13)		mul v1, v0, r1	r5 (▸ p9)	r6 (▸ p10)		
5	4	add v3, v1, v2		r7 (▸ p11)	r9 (▸ p13)	r10 (▸ p14)	ld v2, (r2++)		r6 (▸ p10)	r8 (▸ p12)	
6	3					r11 (▸ p14)			r7 (▸ p10)	r9 (▸ p12)	
7	3					r11 (▸ p14)	add v3, v1, v2		r7 (▸ p10)	r9 (▸ p12)	r10 (▸ p13)
8	2					r12 (▸ p14)					r11 (▸ p13)
9	2	st v3, (r3++)				r12 (▸ p14)					r11 (▸ p13)
10	1										r12 (▸ p13)
11	1						st v3, (r3++)				r12 (▸ p13)

Fig.6A

		Iteration 2					Iteration 3				
Cycle	Offset	Instruction	v0	v1	v2	v3	Instruction	v0	v1	v2	v3
0	6										
1	6										
2	5										
3	5										
4	4	ld v0, (r0++)	r4 (▸ p8)								
5	4		r4 (▸ p8)								
6	3	mul v1, v0, r1	r5 (▸ p8)	r6 (▸ p9)			ld v0, (r0 ++)	r4 (▸ p7)			
7	3	ld v2, (r2++)		r6 (▸ p9)	r8 (▸ p11)			r4 (▸ p7)			
8	2			r7 (▸ p9)	r9 (▸ p11)		mul v1, v0, r1	r5 (▸ p7)	r6 (▸ p8)		
9	2	add v3, v1, v2		r7 (▸ p9)	r9 (▸ p11)	r10 (▸ p12)	ld v2, (r2++)		r6 (▸ p8)	r8 (▸ p10)	
10	1					r11 (▸ p12)			r7 (▸ p8)	r9 (▸ p10)	
11	1					r11 (▸ p12)	add v3, v1, v2		r7 (▸ p8)	r9 (▸ p10)	r10 (▸ p11)
12	0					r12 (▸ p12)					r11 (▸ p11)
13	0	st v3, (r3++)				r12 (▸ p12)					r11 (▸ p11)
14	-1										r12 (▸ p11)
15	-1						st v3, (r3++)				r12 (▸ p11)

Fig.6B

		Iteration 0	Iteration 1	Iteration 2	Iteration 3
Cycle	Offset	Instruction	Instruction	Instruction	Instruction
0	6	ld r4, (r0++)			
1	6				
2	5	mul r6, r5, r1	ld r4, (r0++)		
3	5	ld r8, (r2++)			
4	4		mul r6, r5, r1	ld r4, (r0++)	
5	4	add r10, r7, r9	ld r8, (r2++)		
6	3			mul r6, r5, r1	ld r4, (r0++)
7	3		add r10, r7, r9	ld r8, (r2++)	
8	2				mul r6, r5, r1
9	2	st r14, (r3++)		add r10, r7, r9	ld r8, (r2++)
10	1				
11	1		st r12, (r3++)		add r10, r7, r9
12	0				
13	0			st r12, (r3++)	
14	-1				
15	-1				st r12, (r3++)

Fig.7

		Iteration 0	Iteration 1	Iteration 2	Iteration 3
Cycle	Offset	Instruction	Instruction	Instruction	Instruction
0	6	ld p10, (p0++)			
1	6				
2	5	mul p11, p10, p1	ld p9, (p0++)		
3	5	ld p13, (p2++)			
4	4		mul p10, p9, p1	ld p8, (p0++)	
5	4	add p14, p11, p13	ld p12, (p2++)		
6	3			mul p9, p8, p1	ld p7, (p0++)
7	3		add p13, p10, p12	ld p11, (p2++)	
8	2				mul p8, p7, p1
9	2	st p14, (p3++)		add p12, p9, p11	ld p10, (p2++)
10	1				
11	1		st p13, (p3++)		add p11, p8, p10
12	0				
13	0			st p12, (p3++)	
14	-1				
15	-1				st p11, (p3++)

Fig.8

	Issue slot 1			Issue slot 2			Issue slot 3		
Cycle	Instruction	Iteration	Stage	Instruction	Iteration	Stage	Instruction	Iteration	Stage
0	ld r4, (r0++)	0	1						
1									
2	ld r4, (r0++)	1	1				mul r6, r5, r1	0	2
3	ld r8, (r2++)	0	2						
4	ld r4, (r0++)	2	1				mul r6, r5, r1	1	2
5	ld r8, (r2++)	1	2				add r10, r7, r9	0	3
6	ld r4, (r0++)	3	1				mul r6, r5, r1	2	2
7	ld r8, (r2++)	2	2				add r10, r7, r9	1	3
8							mul r6, r5, r1	3	2
9	ld r8, (r2++)	3	2	st r12, (r3++)	0	5	add r10, r7, r9	2	3
10									
11				st r12, (r3++)	1	5	add r10, r7, r9	3	3
12									
13				st r12, (r3++)	2	5			
14									
15				st r12, (r3++)	3	5			

Fig.9

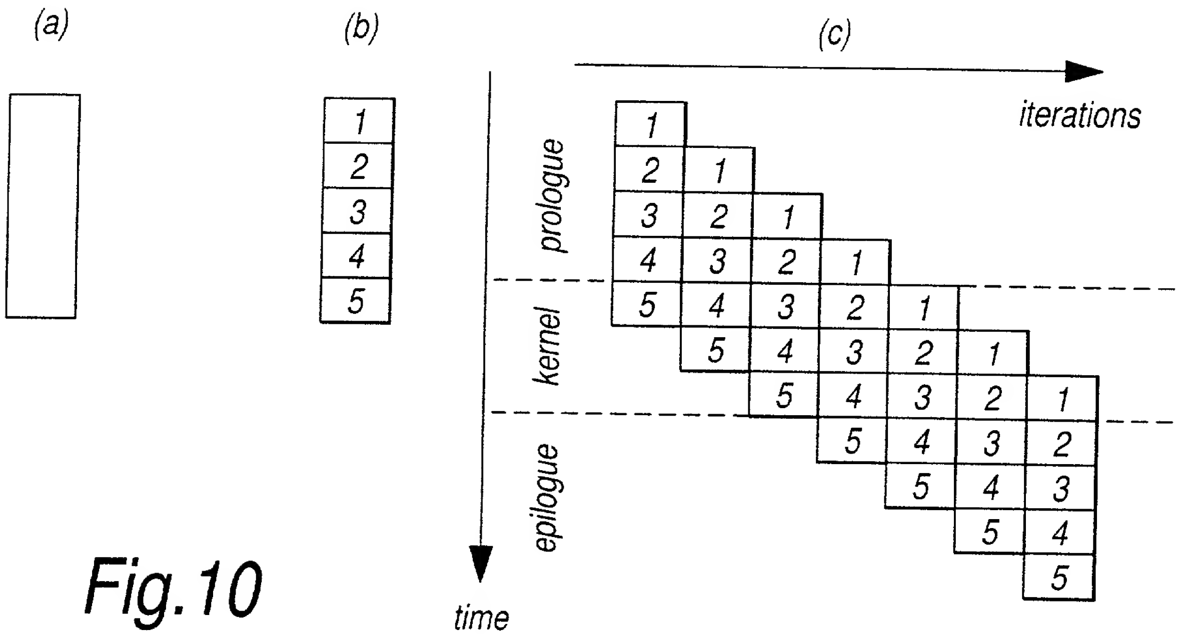
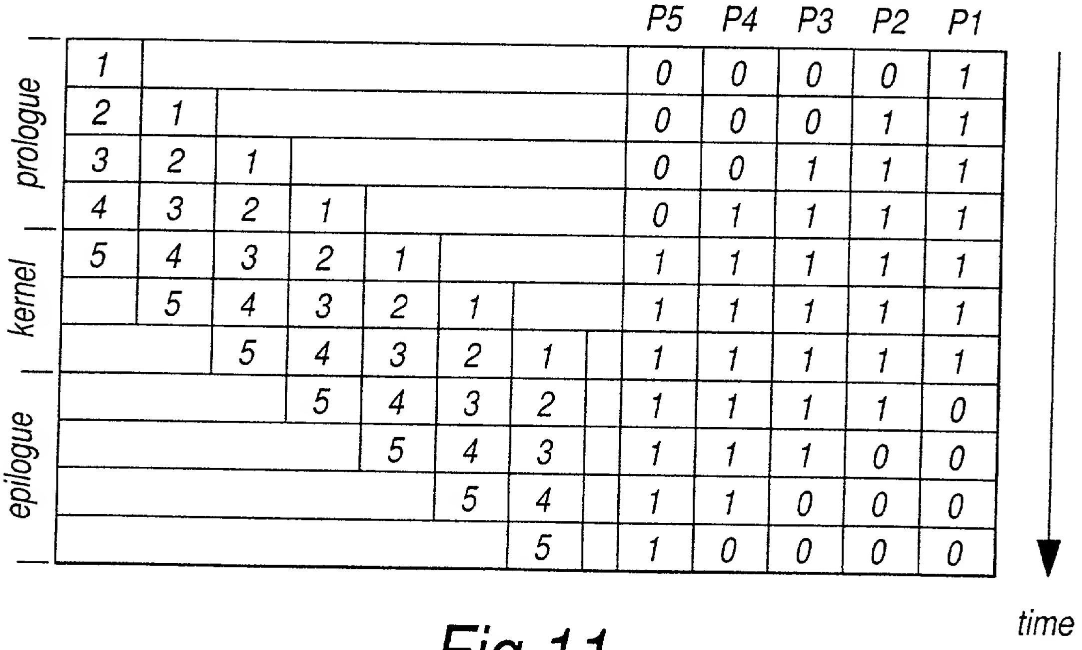


Fig.10



								P5	P4	P3	P2	P1
prologue	1							0	0	0	0	1
	2	1						0	0	0	1	1
	3	2	1					0	0	1	1	1
	4	3	2	1				0	1	1	1	1
kernel	5	4	3	2	1			1	1	1	1	1
		5	4	3	2	1		1	1	1	1	1
			5	4	3	2	1	1	1	1	1	1
epilogue				5	4	3	2	1	1	1	1	0
					5	4	3	1	1	1	0	0
						5	4	1	1	0	0	0
							5	1	0	0	0	0

Fig.11

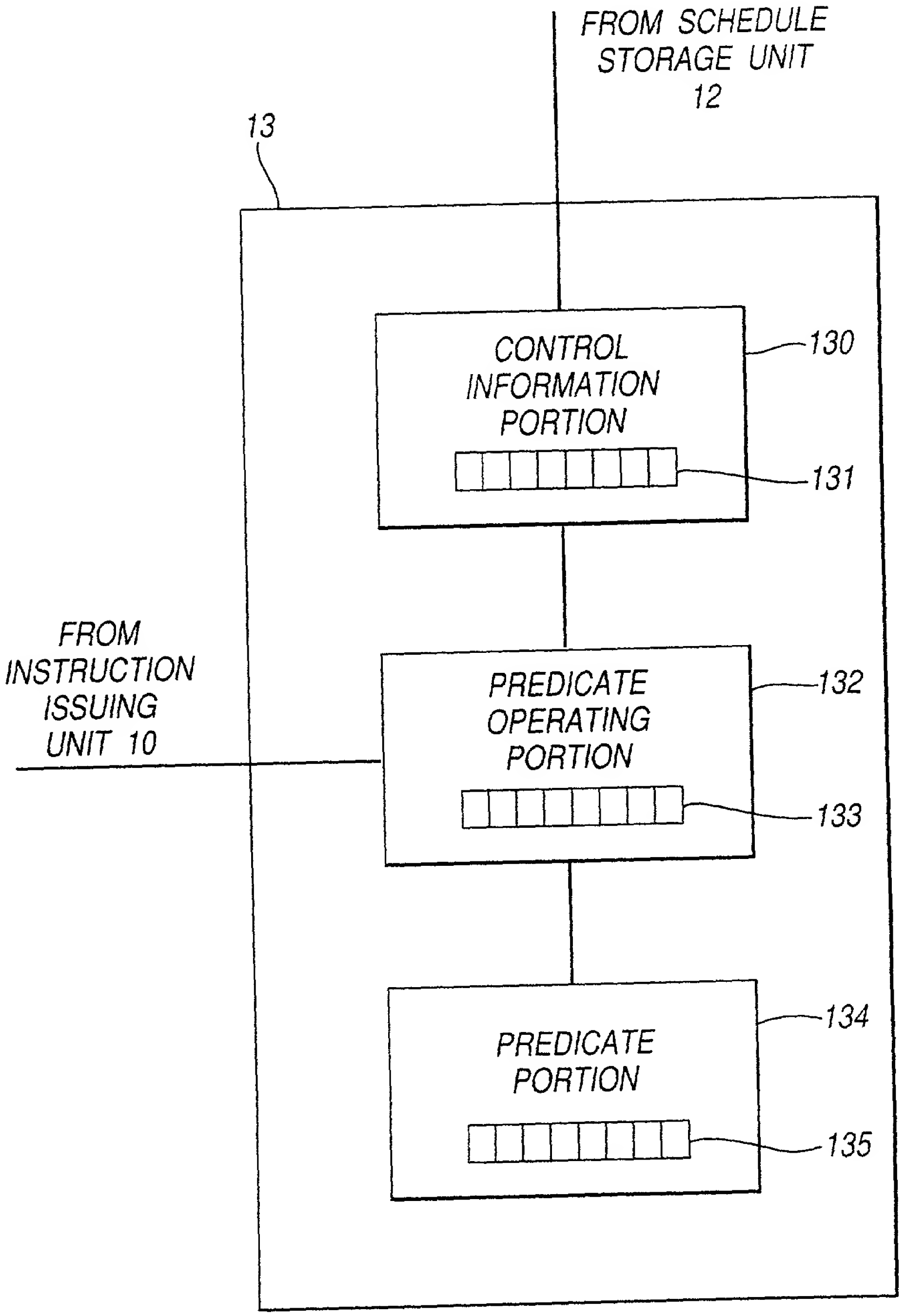

FROM SCHEDULE STORAGE UNIT 12
13
CONTROL INFORMATION PORTION
130
131
FROM INSTRUCTION ISSUING UNIT 10
PREDICATE OPERATING PORTION
132
133
PREDICATE PORTION
134
135

Fig.12

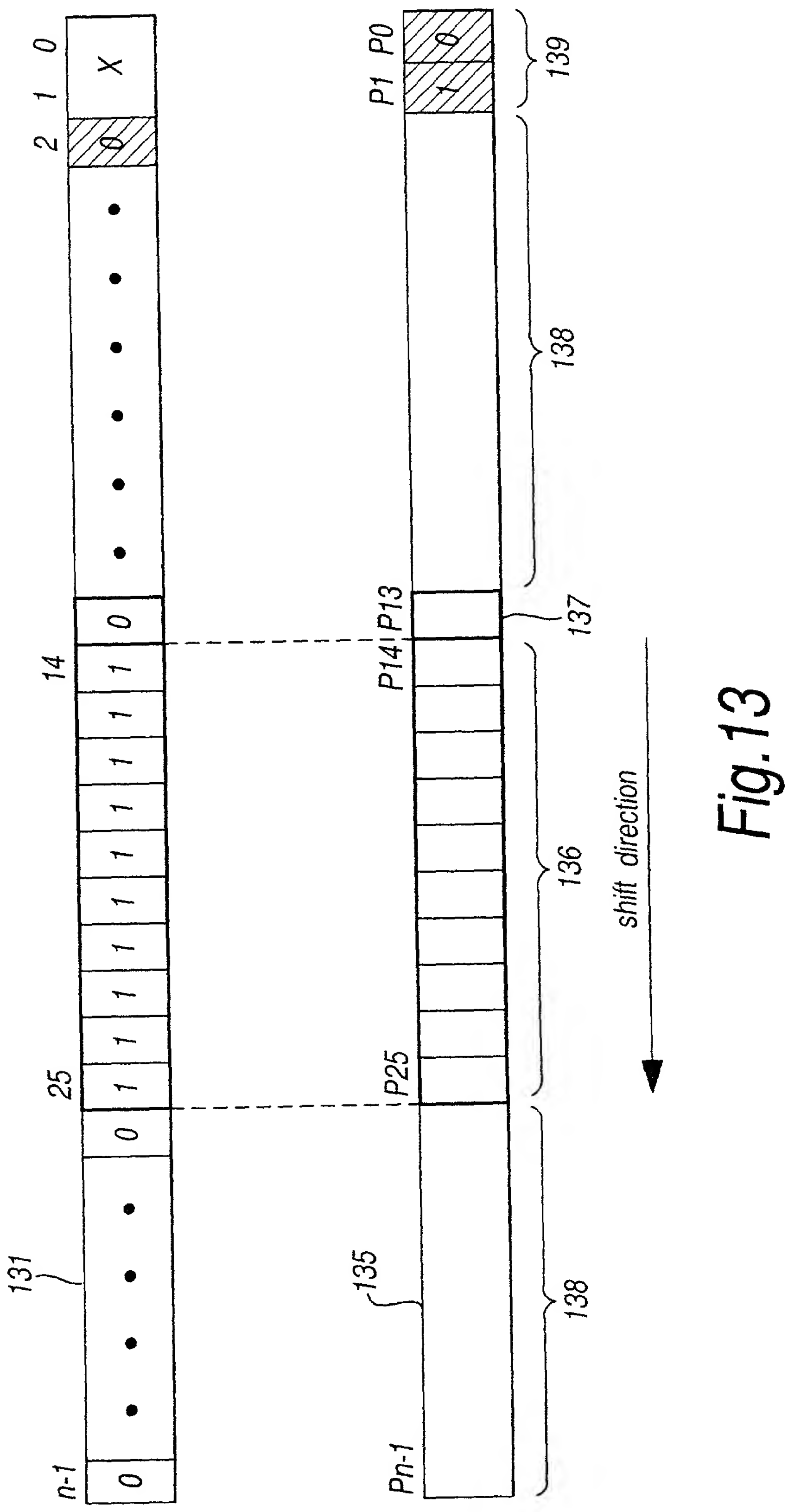

0
1
2
X
0
14
25
0
1
1
1
1
1
1
1
1
1
1
1
1
0
131
n-1
0
P0
P1
0
1
139
138
P13
137
P14
136
P25
135
Pn-1
138
shift direction

Fig.13

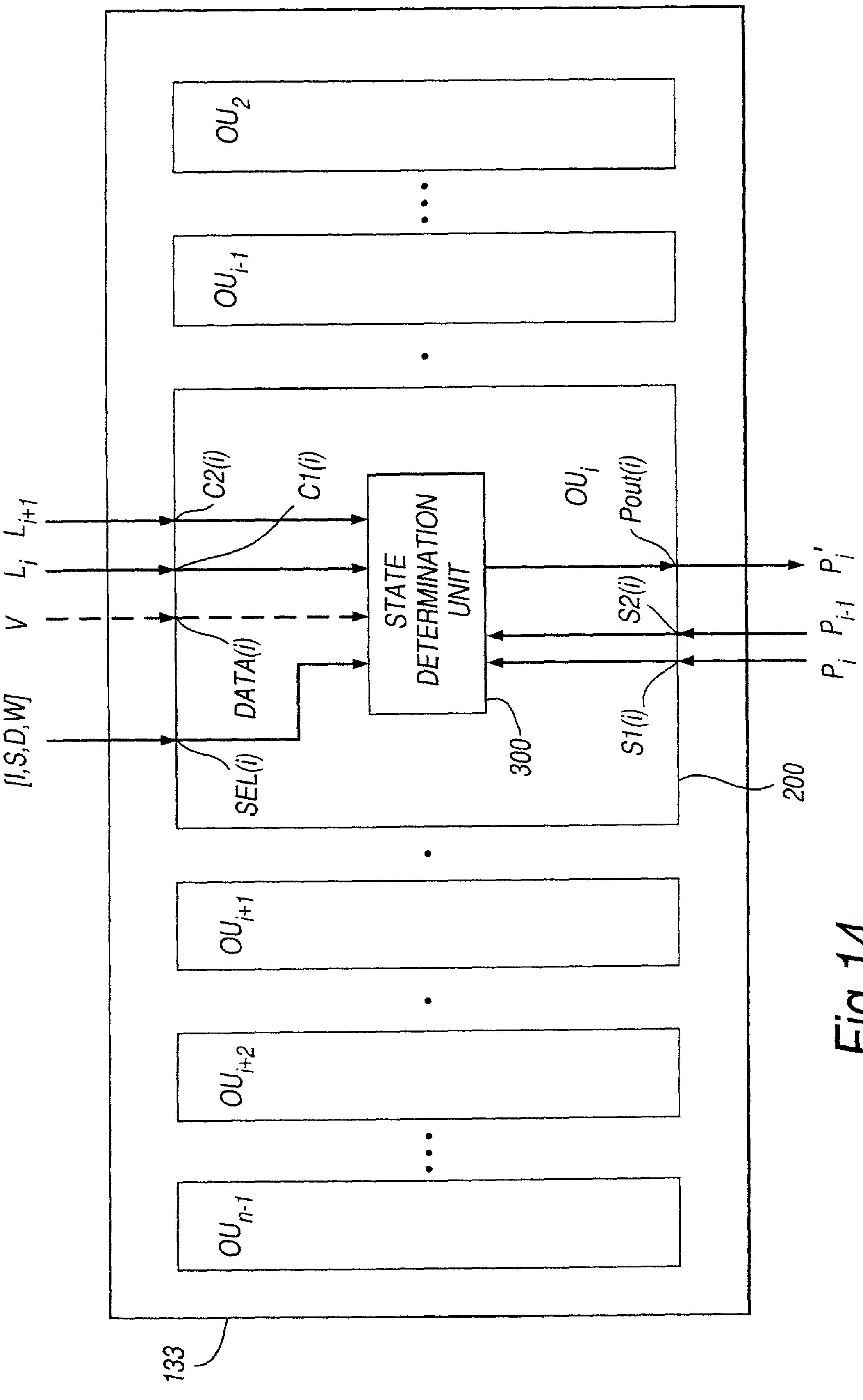

OU$_2$
OU$_{i-1}$
OU$_i$
STATE DETERMINATION UNIT
C2(i)
C1(i)
Pout(i)
S2(i)
S1(i)
DATA(i)
SEL(i)
300
200
L_{i+1}
L_i
V
[I,S,D,W]
P_i'
P_{i-1}
P_i
OU$_{i+1}$
OU$_{i+2}$
OU$_{n-1}$
133

Fig.14

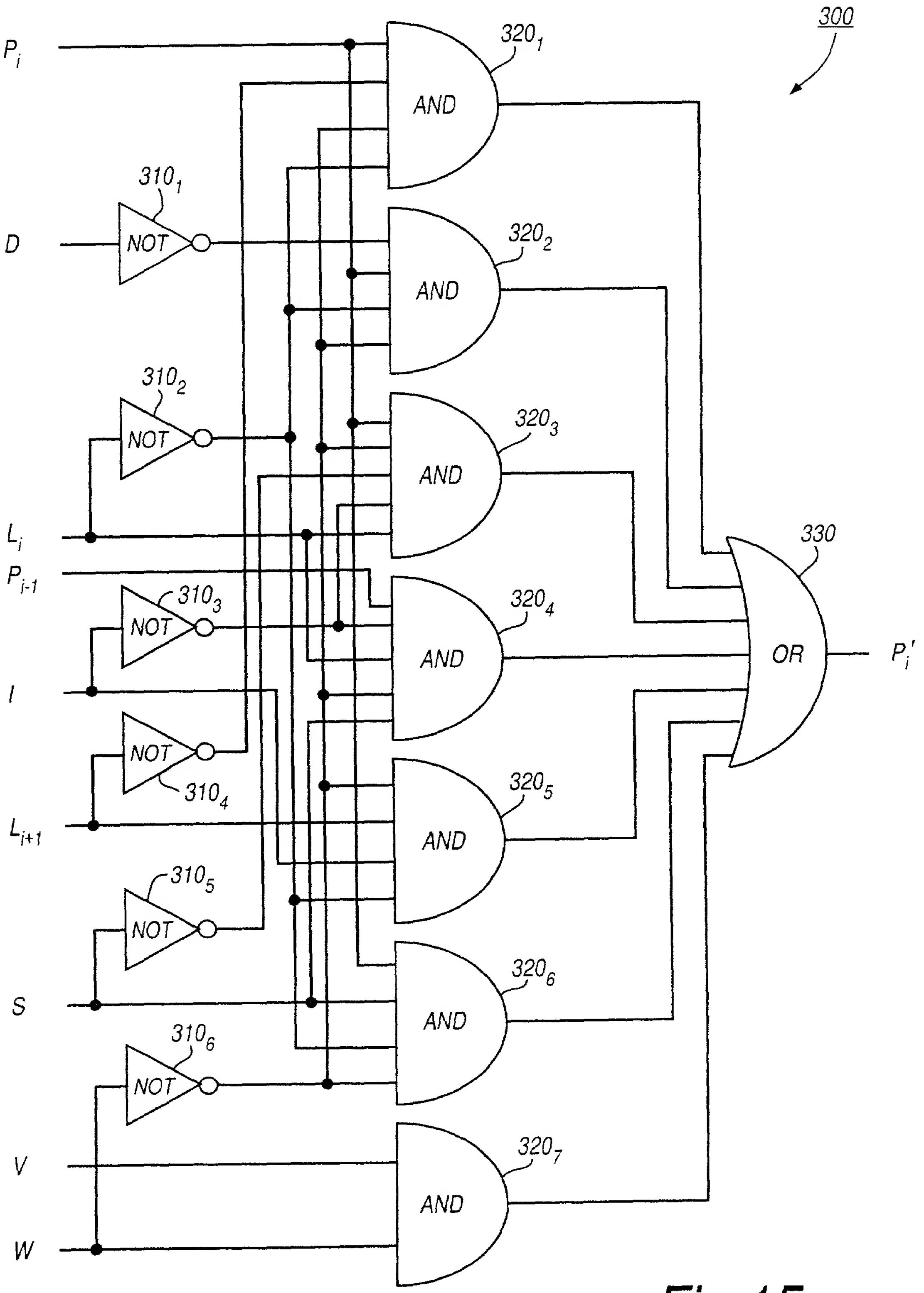

300
P_i
D
L_i
P_{i-1}
I
L_{i+1}
S
V
W
310_1
310_2
310_3
310_4
310_5
310_6
NOT
NOT
NOT
NOT
NOT
NOT
320_1
320_2
320_3
320_4
320_5
320_6
320_7
AND
AND
AND
AND
AND
AND
AND
330
OR
P_i'

Fig.15

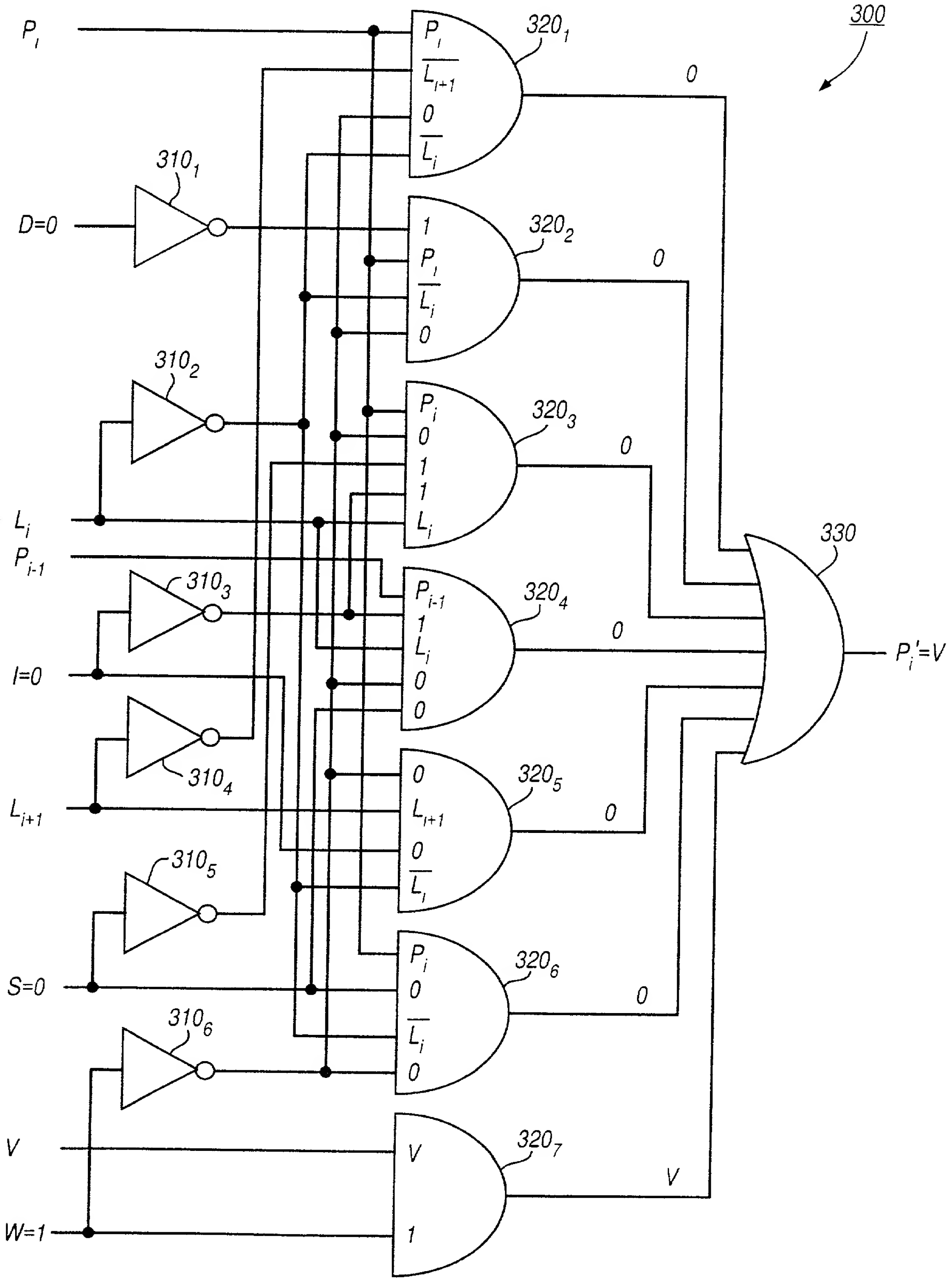

300
P_i
D=0
L_i
P_{i-1}
I=0
L_{i+1}
S=0
V
W=1
310_1
310_2
310_3
310_4
310_5
310_6
320_1
P_i
$\overline{L_{i+1}}$
0
$\overline{L_i}$
320_2
1
P_i
$\overline{L_i}$
0
320_3
P_i
0
1
1
L_i
320_4
P_{i-1}
1
L_i
0
0
320_5
0
L_{i+1}
0
$\overline{L_i}$
320_6
P_i
0
$\overline{L_i}$
0
320_7
V
1
0
0
0
0
0
0
V
330
$P_i'=V$

Fig.16

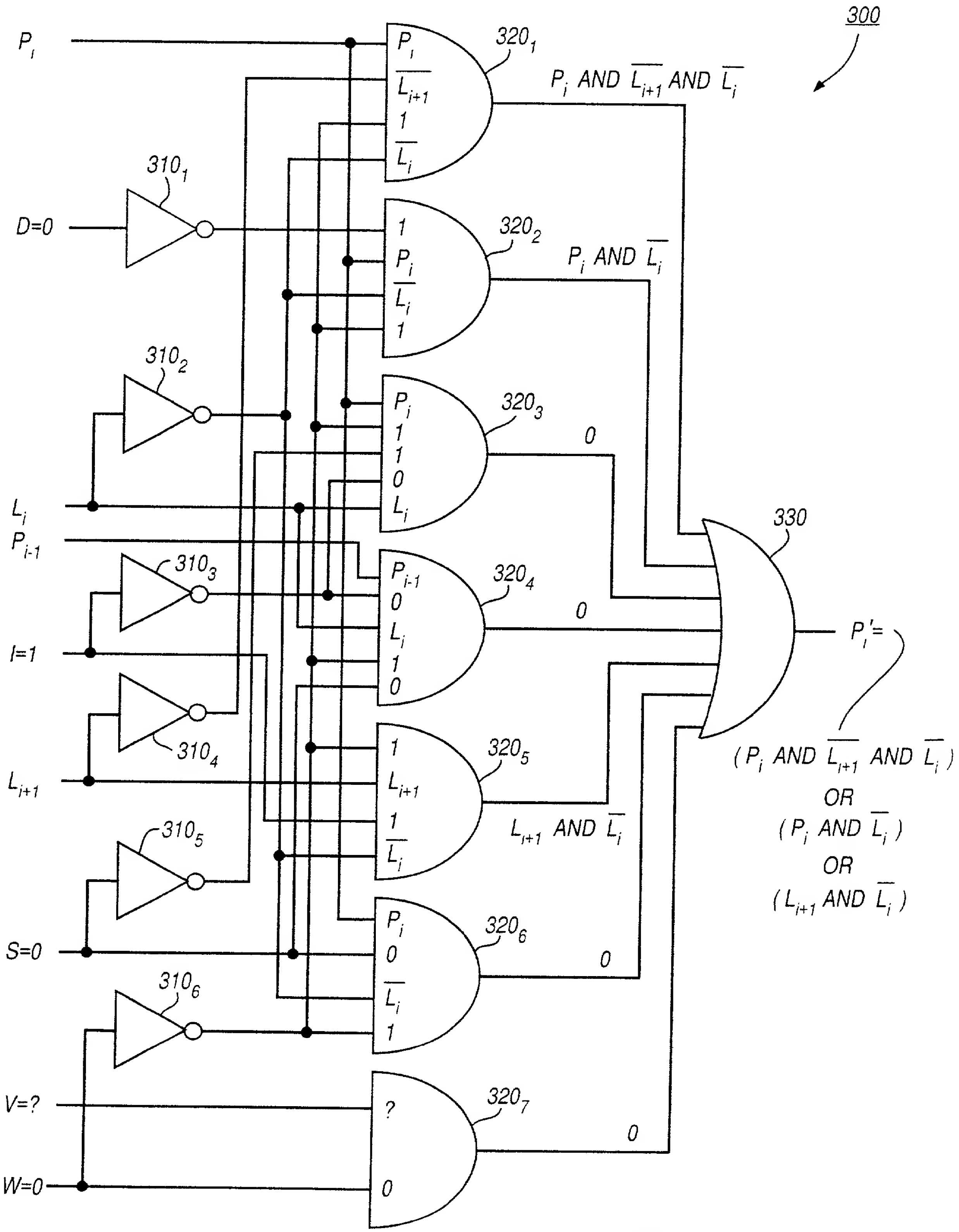

300
P_i
320_1
P_i
$\overline{L_{i+1}}$
1
$\overline{L_i}$
P_i AND $\overline{L_{i+1}}$ AND $\overline{L_i}$
310_1
D=0
1
P_i
$\overline{L_i}$
1
320_2
P_i AND $\overline{L_i}$
310_2
P_i
1
1
0
L_i
320_3
0
L_i
P_{i-1}
310_3
P_{i-1}
0
L_i
1
0
320_4
0
330
I=1
P_i'=
310_4
L_{i+1}
1
L_{i+1}
1
$\overline{L_i}$
320_5
L_{i+1} AND $\overline{L_i}$
(P_i AND $\overline{L_{i+1}}$ AND $\overline{L_i}$)
OR
(P_i AND $\overline{L_i}$)
OR
(L_{i+1} AND $\overline{L_i}$)
310_5
S=0
P_i
0
$\overline{L_i}$
1
320_6
0
310_6
V=?
?
320_7
0
W=0
0

Fig.17

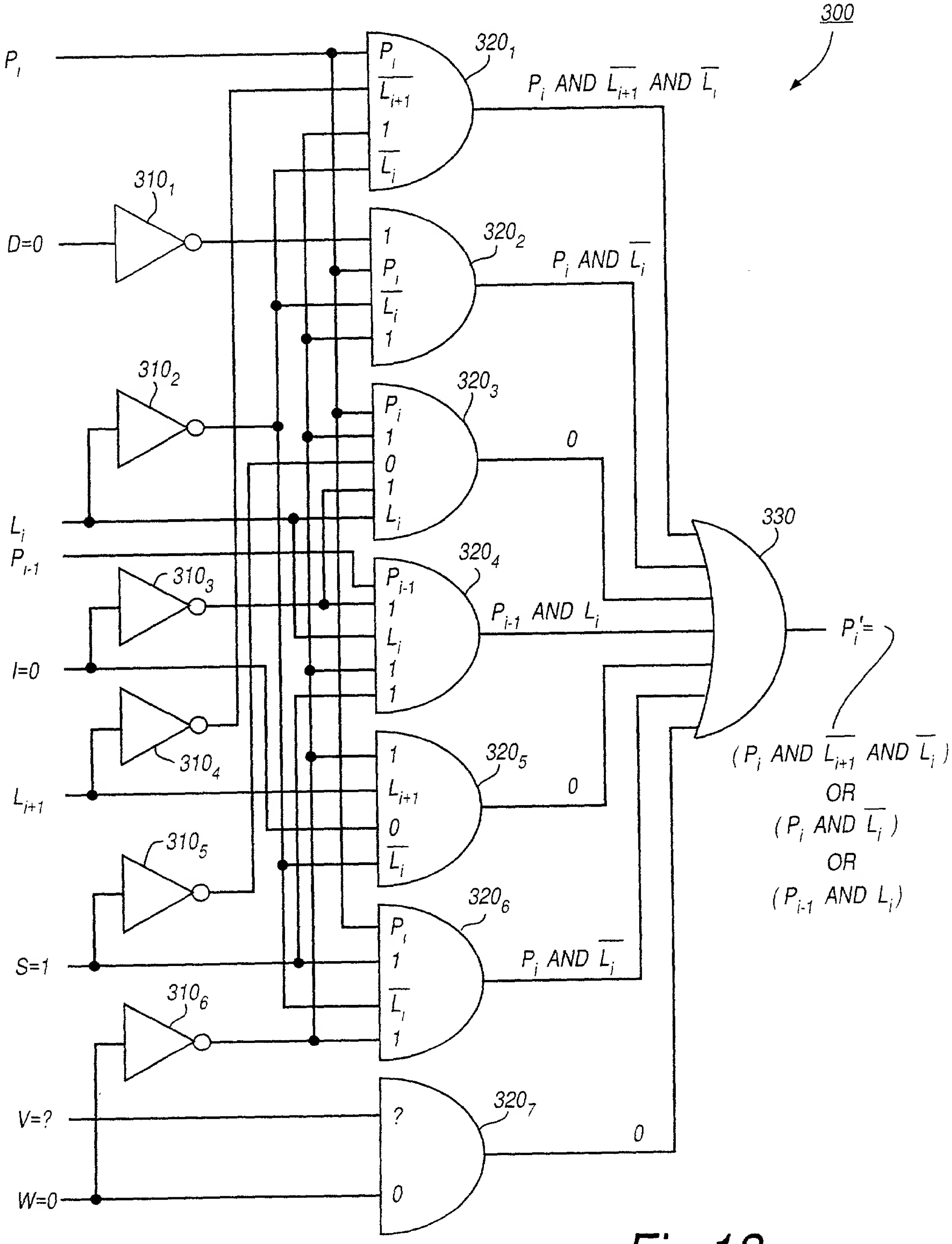

300
P_i
$D=0$
L_i
P_{i-1}
$I=0$
L_{i+1}
$S=1$
$V=?$
$W=0$
310_1
310_2
310_3
310_4
310_5
310_6
320_1
P_i, $\overline{L_{i+1}}$, 1, $\overline{L_i}$
P_i AND $\overline{L_{i+1}}$ AND $\overline{L_i}$
320_2
1, P_i, $\overline{L_i}$, 1
P_i AND $\overline{L_i}$
320_3
P_i, 1, 0, 1, L_i
0
320_4
P_{i-1}, 1, L_i, 1, 1
P_{i-1} AND L_i
320_5
1, L_{i+1}, 0, $\overline{L_i}$
0
320_6
P_i, 1, $\overline{L_i}$, 1
P_i AND $\overline{L_i}$
320_7
?, 0
0
330
$P_i'=$
(P_i AND $\overline{L_{i+1}}$ AND $\overline{L_i}$)
OR
(P_i AND $\overline{L_i}$)
OR
(P_{i-1} AND L_i)

Fig.18

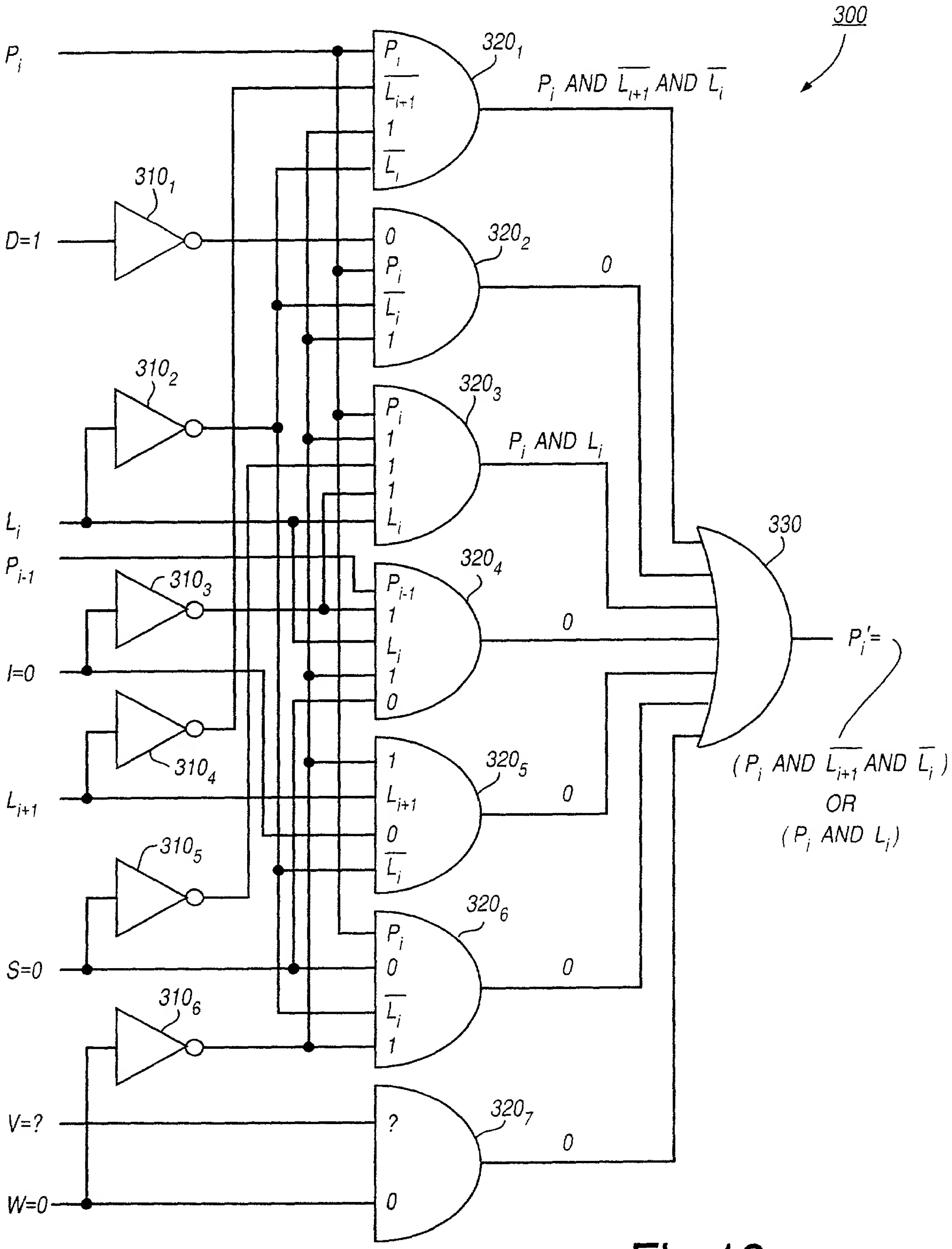

300
P_i
D=1
L_i
P_{i-1}
I=0
L_{i+1}
S=0
V=?
W=0
310_1
310_2
310_3
310_4
310_5
310_6
320_1
P_i
$\overline{L_{i+1}}$
1
$\overline{L_i}$
P_i AND $\overline{L_{i+1}}$ AND $\overline{L_i}$
320_2
0
P_i
$\overline{L_i}$
1
0
320_3
P_i
1
1
1
L_i
P_i AND L_i
320_4
P_{i-1}
1
L_i
1
0
0
320_5
1
L_{i+1}
0
$\overline{L_i}$
0
320_6
P_i
0
$\overline{L_i}$
1
0
320_7
?
0
0
330
P_i'=
(P_i AND $\overline{L_{i+1}}$ AND $\overline{L_i}$)
OR
(P_i AND L_i)

Fig.19